0.151 microns and 0.169 microns. The final after etch polysilicon CD is specified at between about 0.145 microns and 0.125 microns. Since the final polysilicon CD is about 0.025 microns less than the available resist CD, it is necessary to trim back the width of the resist layer **80**.

The trimming etch recipe preferably comprises a combination of gases. In the preferred embodiment, HBr gas is flowing at a rate of between about 60 sccm and 100 sccm, Ar gas is flowing at a rate of between about 40 sccm and 80 sccm, and O_2 gas is flowing at a rate of between about 2 sccm and 10 sccm. The chamber pressure is between about 4 milliTorr and 15 milliTorr. A source power of between about 200 Watts and 400 Watts and a bias power of between about 40 Watts and 80 Watts are used. The trimming etch is performed for between about 20 seconds and 60 seconds. The trimming etch reduces the width of the resist layer **80** prior to transferring the pattern to the hard mask layer **72**.

Following the trim etch, the hard mask layer **72** is etched. If the silicon dioxide layer **76** is used, it is etched with the hard mask layer. The hard mask etch comprises a combination of gases. In the preferred embodiment, CF_4 gas is flowing at a rate of between about 10 sccm and 30 sccm and Ar gas is flowing at a rate of between about 140 sccm and 160 sccm. The chamber pressure is maintained at between about 8 milliTorr and 12 milliTorr. The source power is controlled at between about 550 Watts and 650 Watts while the bias power is controlled at between about 40 Watts and 80 Watts. The hard mask layer **72** is etched using an endpoint detection that detects when the hard mask layer **72** has been etched through.

Following the hard mask etch, the resist layer **80** is stripped away. The ability to perform this step within the same dry etch plasma chamber is an important feature of the present invention. The resist layer **80** is removed by flowing O_2 gas at a rate of between about 40 sccm and 60 sccm. A chamber pressure of between about 4 milliTorr and 15 milliTorr is maintained. The source power is controlled at between about 300 Watts and 500 Watts, while the bias power is controlled at between about 80 Watts and 100 Watts. The strip is stopped using an endpoint detection that detects that the photoresist layer **80** is no longer present.

Following the resist strip step, it is likely that organic polymer residue remains from the photoresist material. This residue will coat the interior of the dry plasma etching chamber and may adhere to the sidewalls of the hard mask **72** and **76** as shown by **84** in FIG. **10**. It is critical to the method of the present invention that the resist stripping step be followed by a polymer cleaning step. The polymer clean removes any organic polymer residue from the chamber and from the sidewalls of the hard mask **72** and **76**.

The polymer clean step is accomplished by flowing CF_4 gas at a rate of between about 60 sccm and 100 sccm. The chamber pressure is maintained at between about 4 milliTorr and 15 milliTorr. The source power is controlled at between about 300 Watts and 500 Watts, while the bias power is controlled at between about 30 Watts and 50 Watts. The polymer clean is performed for between about 5 seconds and 15 seconds. The polymer cleaning step keeps the chamber clean prior to each polysilicon etch process.

Referring now to FIG. **11**, the polysilicon layer **68** is now etched using two recipe steps comprising, first, a main etch (ME) and, second, an overetch (OE). In the main etch, the polysilicon layer **68** is etched using a gas combination of HBr, Cl_2, and He—O_2. The main etch is stopped using an endpoint detection method that detects when the polysilicon layer **68** has been etched through. The overetch recipe uses a gas combination of HBr and He—O_2 for a controlled time period to insure that the remaining polysilicon layer **68** will be free of stringers and shorts.

The main etch comprises HBr flowing at a rate of between about 160 sccm and 200 sccm, Cl_2 flowing at a rate of between about 10 sccm and 30 sccm, and He—O_2 flowing at a rate of between about 2 sccm and 10 sccm. The chamber pressure is maintained at between about 4 milliTorr and 15 milliTorr. The source power is controlled at between about 550 Watts and 650 Watts. The bias power is controlled at between about 30 Watts and 50 Watts.

The overetch recipe comprises HBr flowing at a rate of between about 130 sccm and 150 sccm and He—O_2 flowing at a rate of between about 4 sccm and 6 sccm. The chamber pressure is maintained at between about 60 milliTorr and 100 milliTorr. The source power is controlled at between about 300 Watts and 500 Watts, while the bias power is controlled at between about 60 Watts and 80 Watts. The overetch is performed for between about 60 seconds and 100 seconds. Following the polysilicon etch, the device cross-section appears as shown in FIG. **11**. The silicon dioxide layer **76** is etched away during the polysilicon etch step.

Referring now to FIG. **12**, the hard mask is stripped away to complete the patterning of the polysilicon layer **68**. The wafers are removed from the dry plasma etch chamber to perform the hard mask strip. In the preferred embodiment, the hard mask layer **72** comprises silicon oxynitride. This silicon oxynitride layer **72** is preferably removed using a wet etch comprising H_3PO_4.

The method of the present invention, using the in-situ stripping of the photoresist layer, has been demonstrated on a 0.15 micron process. The method demonstrates stable after etch inspection (AEI) CD performance. The three-sigma variation is between about 4 nanometers and 8 nanometers. SEM and X-SEM profiles, after polysilicon gate etching, demonstrate excellent vertical profiles with no pitting, trenching, or residue problems. In addition, the method saves about 4 hours compared to the prior art approach.

As shown in the preferred embodiments, the present invention provides a very manufacturable process for patterning the polysilicon layer in an integrated circuit device. The present invention saves cycle time and reduces costs. The present invention has been successfully demonstrated on a 0.15 micron process. The novel approach allows photoresist to be stripped away in the dry plasma etch chamber. The polymer cleaning step eliminates problems associated with resist residue build-up in the chamber or on hard mask sidewalls.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a polysilicon layer overlying a semiconductor substrate;

providing a hard mask layer overlying said polysilicon layer;

providing a resist layer overlying said hard mask layer;

patterning said resist layer to form a resist mask that exposes a part of said hard mask layer;

patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said hard mask layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said hard mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by said hard mask; and

stripping away said hard mask to complete the patterning of said polysilicon layer in the manufacture of the integrated circuit device.

2. The method according to claim 1 wherein said hard mask layer comprises silicon oxynitride.

3. The method according to claim 1 wherein said step of etching said hard mask layer comprises a chemistry containing CF_4 gas.

4. The method according to claim 1 wherein said step of stripping away said resist mask comprises a chemistry containing O_2 gas.

5. The method according to claim 1 wherein said step of etching said polysilicon layer comprises a main etch step followed by an overetch step.

6. The method according to claim 1 wherein said step of etching said polysilicon layer comprises a chemistry of: HBr gas, Cl_2 gas, He—O_2 gas, and combinations thereof.

7. The method according to claim 1 further comprising providing a silicon dioxide layer overlying said hard mask layer and underlying said resist layer.

8. The method according to claim 1 further comprising etching said resist layer to trim said resist layer prior to said step of etching said hard mask layer wherein said etching of said resist layer is performed in said dry plasma etching chamber.

9. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a polysilicon layer overlying a semiconductor substrate;

providing a hard mask layer overlying said polysilicon layer;

providing a silicon dioxide layer overlying said hard mask layer;

providing a resist layer overlying said hard mask layer;

patterning said resist layer to form a resist mask that exposes a part of said hard mask layer;

patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said resist mask to trim said resist mask;

thereafter etching said hard mask layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said resist mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by said hard mask; and

stripping away said hard mask to complete the patterning of said polysilicon layer in the manufacture of the integrated circuit device.

10. The method according to claim 9 wherein said hard mask layer comprises silicon oxynitride.

11. The method according to claim 9 wherein said step of etching said resist mask to trim said resist mask comprises a chemistry containing O_2 gas.

12. The method according to claim 9 wherein said step of etching said hard mask layer comprises a chemistry of CF_4 gas.

13. The method according to claim 9 wherein said step of stripping away said resist layer comprises a chemistry containing O_2 gas.

14. The method according to claim 9 wherein said step of etching said polysilicon layer comprises a main etch step followed by an overetch step.

15. The method according to claim 9 wherein said step of etching said polysilicon layer comprises a chemistry of: HBr gas, Cl_2 gas, He—O_2 gas, and combinations thereof.

16. A method to pattern a polysilicon layer in the manufacture of an integrated circuit device comprising:

providing a gate oxide layer overlying a semiconductor substrate;

providing a polysilicon layer overlying said gate oxide layer;

providing a silicon oxynitride layer overlying said polysilicon layer;

providing a silicon dioxide layer overlying said silicon oxynitride layer;

providing a resist layer overlying said silicon dioxide layer;

patterning said resist layer to form a resist mask that exposes a part of said silicon dioxide layer;

patterning said polysilicon layer wherein said patterning is performed sequentially in a dry plasma etch chamber and wherein said patterning comprises:

etching said resist mask to trim said resist mask;

thereafter etching said silicon dioxide layer and said silicon oxynitride layer exposed by said resist mask to form a hard mask that exposes a part of said polysilicon layer;

thereafter stripping away said resist mask;

thereafter cleaning away polymer residue from said resist mask wherein said cleaning away comprises a chemistry containing CF_4 gas; and

thereafter etching said polysilicon layer exposed by said hard mask wherein said etching comprises a main etch step followed by an overetch step; and

stripping away said hard mask to complete the patterning of said polysilicon layer in the manufacture of the integrated circuit device.

17. The method according to claim 16 wherein said step of etching said silicon dioxide layer and said silicon oxynitride layer comprises a chemistry of CF_4 gas.

18. The method according to claim 16 wherein said step of stripping away said resist layer comprises a chemistry containing O_2 gas.

19. The method according to claim 16 wherein said step of etching said polysilicon layer comprises a chemistry of: HBr gas, Cl_2 gas, He—O_2 gas, and combinations thereof.

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